Key Recovery from Side-Channel Power Analysis Attacks on Non-SIMD HQC Decryption

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Correlated power consumption variations and secrets make the power consumption monitoring sensitive.

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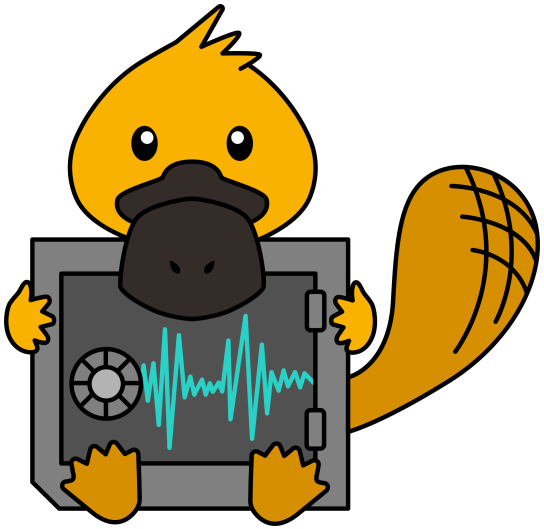
- Takes advantage of Intel RAPL
- Breaks KASLR, leak AES-NI keys...
- CVE-2020-{8694, 8695}: CVSS 5.5



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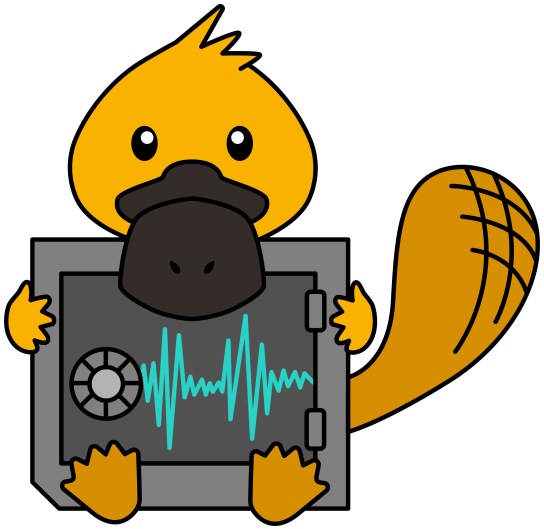
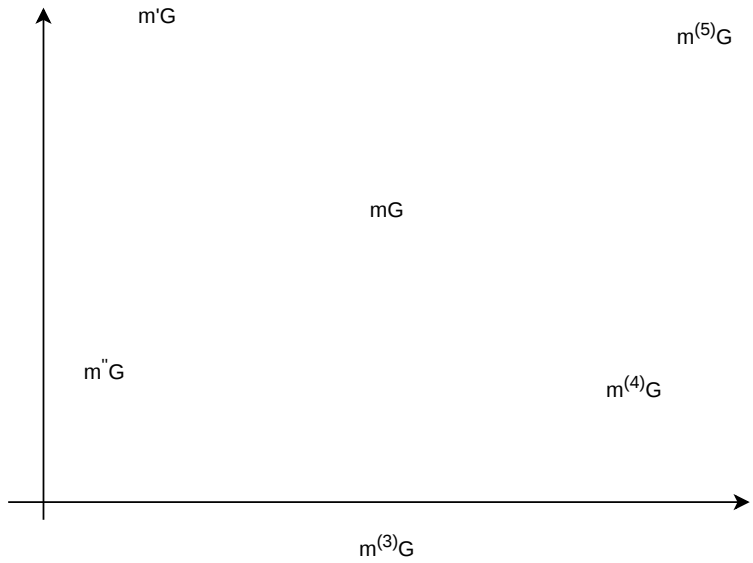


Hertzbleed

- Power to timing SCA using DVFS
- Breaks a lot of crypto, pixel stealing attacks...
- CVE-2022-{23823, 24436, 35888}: CVSS 6.5

TL;DR of HQC



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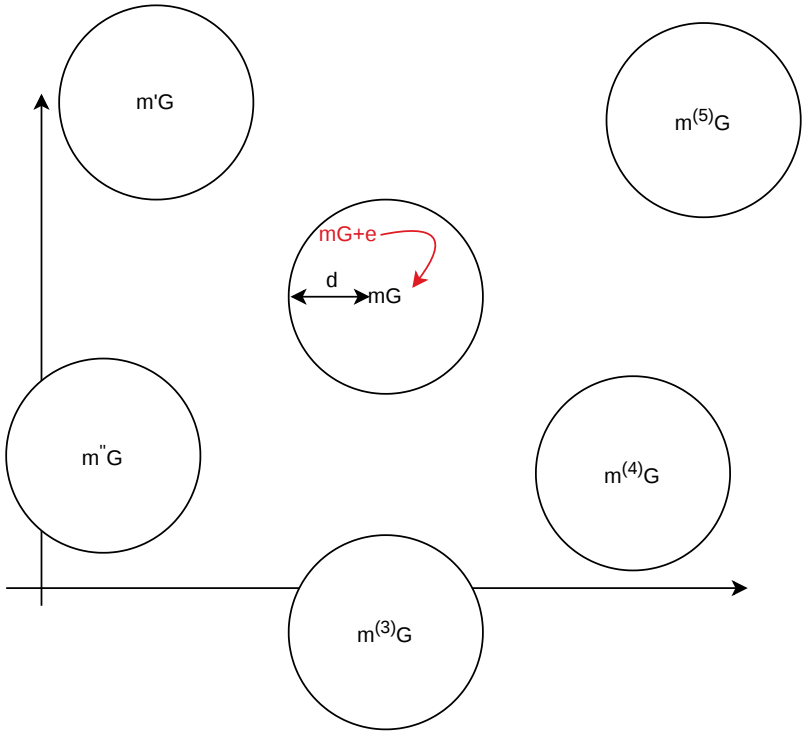

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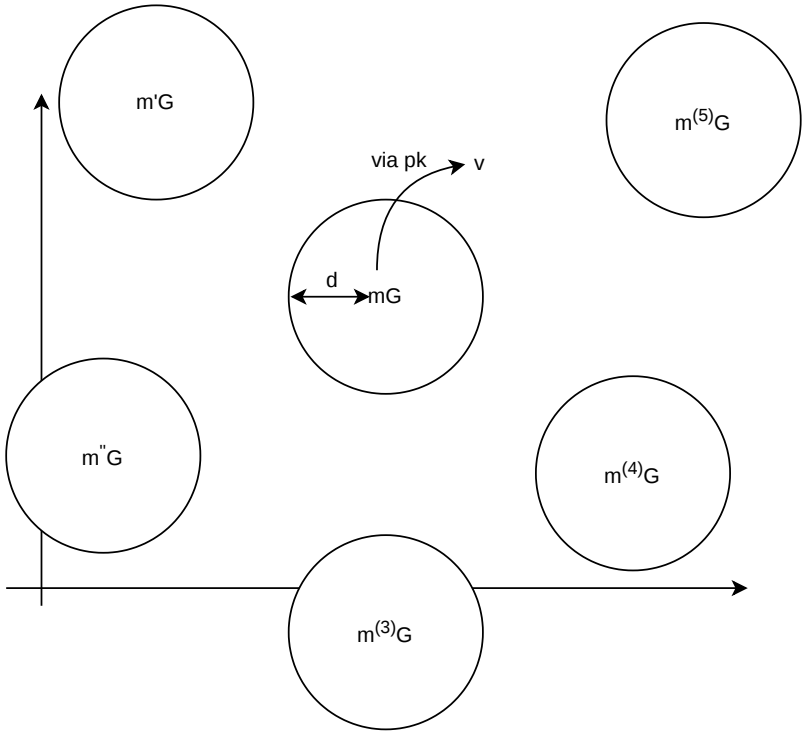

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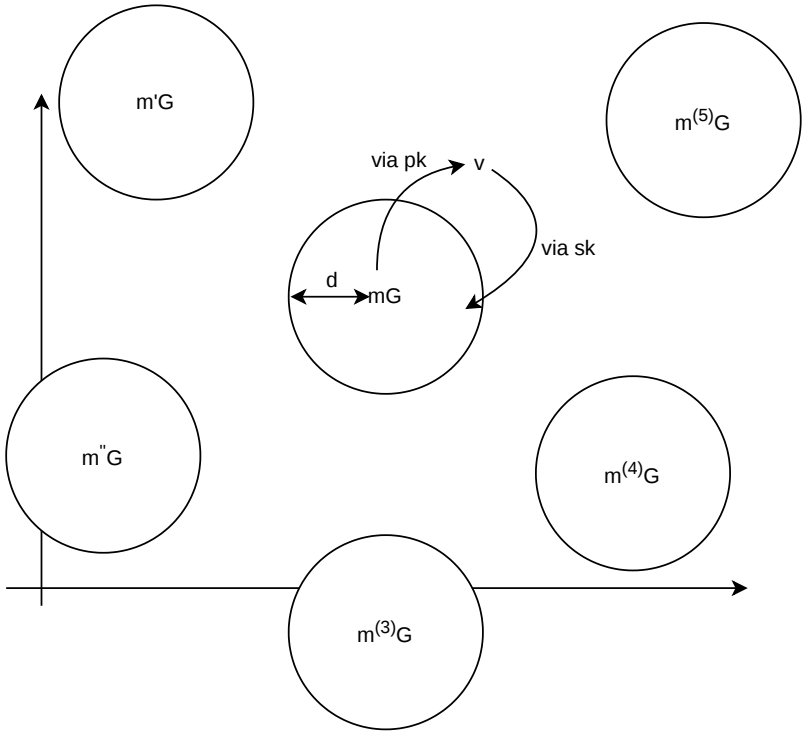
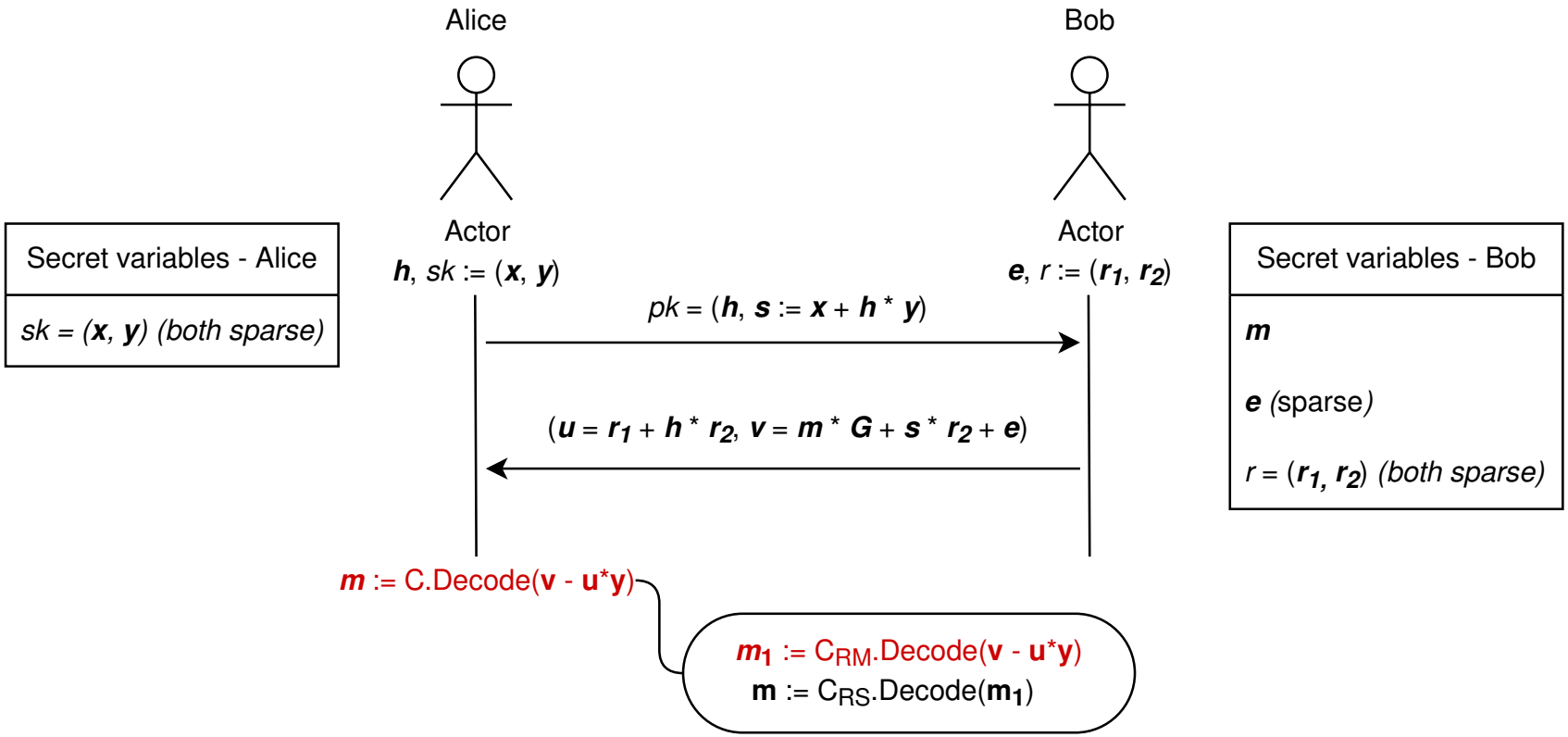


HQC as a KEM



Remarks

- HQC's code uses Reed-Muller (RM) and Reed-Solomon (RS) codes and works on vectors of Hamming Weight $\approx \sqrt{n}$, n being the length of the code.
- Any vector can be viewed as a polynomial of $\mathcal{R} = \mathbb{F}_2[X]/(X^n - 1)$.

What did we do with HQC?

Sum-up of our contributions

- Two Side-Channel Attacks on the SIMD-less implementation of HQC targeting the duplicated-RM decoding:
  - An ISA-level attack needing only 1 oracle call
  - A replay attack on a Cortex-M4 microarchitecture
- Countermeasures to our attacks which can be applied as countermeasures to other known attacks.

Why would we want to remove the SIMD?

Usage

SIMD-less implementation represents a *portable*, *IoT-friendly* version, close to what would be used in production.

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Version of HQC	Cycle count (mean)	Cycle count (std)
Optimized (SIMD -O3)	471	72
SIMD -O2	550	239
No SIMD	312	12
Reference	669	58

Table: Performances of the attacked function (`expand_and_sum`) for diverse implementations of HQC

Comparison of this work with known attacks on HQC

Attack	Oracle calls	HQC implem.	Type of SCA
[this work]	1	Optimized, no SIMD	⚡
[TCHES:GMGL24]	1	Reference	🧲
[USENIX:SchGasGuo24]	1142	Optimized	🕰
[TCHES:HSCGJ23; AC:GNNJ23]	9000	Reference	🕰
[TCHES:GHJLNS22; AC:GNNJ23]	10000	Optimized	🕰
[PQCRYPTO:SHRWS22]	52992	Reference	⚡
[TCHES:HSCGJ23]	53857	Reference	🕰
[TCHES:GHJLNS22]	866000	Optimized	🕰

Table: Oracle calls needed for each ISA-level attack on HQC-128

Two Side-Channel Attacks targeting the duplicated-RM decoding

An ISA-level attack needing only 1 oracle call

ISA	Optimization flag					
	-Og	-O0	-O1	-O2	-O3	-Oz
RISC-V	V0/V1	V0/V1	V0/V1	V0/V1	V0/V1	-
AArch32	V0/V1	V0/V1	V0/V1	V0/V1	V0/V1	V0/V1
x86-64	V0/V1	V0/V1	V1	V1	V1	V1

Table: Applicability of the ISA-level attack for both of our variants

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AArch32	V0/V1	V0/V1	V0/V1	V0/V1	V0/V1	V0/V1
x86-64	V0/V1	V0/V1	V1	V1	V1	V1

Table: Applicability of the ISA-level attack for both of our variants

A replay attack on a Cortex-M4 microarchitecture

83 (resp. 56) traces are enough to ensure a key recovery with 99% (resp. 50%) for any HQC version.

Countermeasures to those attacks

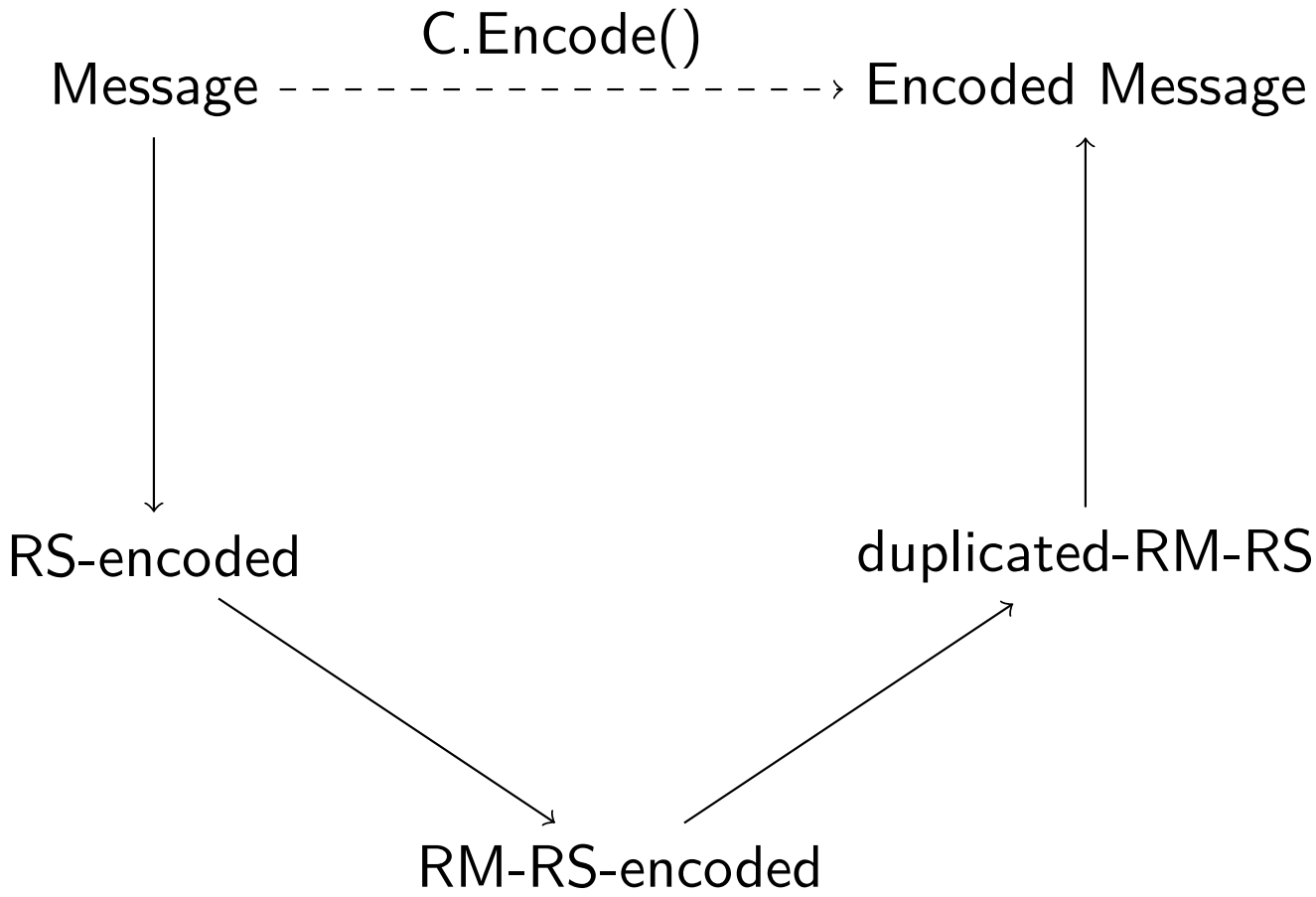
Attack \ Countermeasure	Min. Dist. Decoding	Adding Noise	Code-word masking*
[this work]	✓	✓	✓
[TCHES:GMGL24]	×	×	✓
[USENIX:SchGasGuo24]	×	✓	✓
[PQCRYPTO:SHRWS22]	×	✓	×
[TCHES:HSCGJ23]	×	×	×
[TCHES:GHJLNS22]	×	×	×

Table: Effectiveness of our countermeasures for each known attack

*Under the assumption of a leakage-free codeword masking.

Code used in HQC

HQC's Encoding



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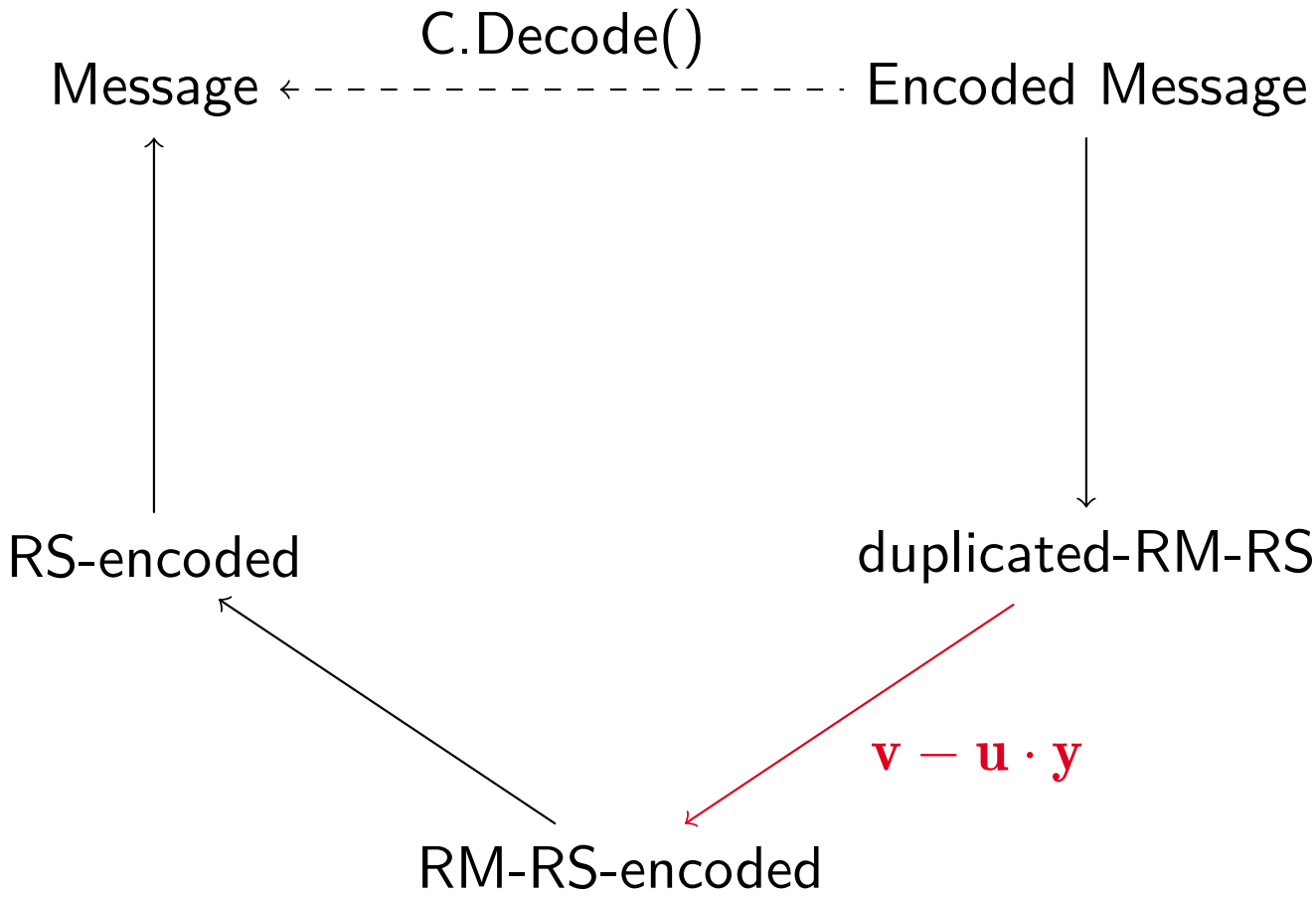

From leakage to the secret key

Assuming $\mathbf{v} - \mathbf{u} \cdot \mathbf{y}$ is known by SCA, and $\mathbf{u}$ is invertible, we have:

$$\mathbf{y} = \mathbf{u}^{-1} \cdot (\mathbf{v} - (\mathbf{v} - (\mathbf{u} \cdot \mathbf{y}))), \text{ and thus, } \mathbf{x} = \mathbf{s} - \mathbf{h} \cdot \mathbf{y}$$

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Theorem (Security reduction)

$\forall\, \mathbf{u}$, *a brute-force of* $n - \mathbf{rk}(\mathbf{rot}(\mathbf{u}))$ *bits is enough to recover* $\mathbf{y}$.

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Theorem (Specifity of $\mathbf{u}$)

Let $\mathbf{u} \in \mathcal{R}$ *and* $\mathbb{1} = 1 + X + \cdots + X^{n-1}$. *The following holds:*

$$\mathbf{rk}(\mathbf{rot}(u)) = \begin{cases} 0 & \text{if } \mathbf{u} = 0 \\ 1 & \text{if } \mathbf{u} = \mathbb{1} \\ n-1 & \text{if } \mathbf{u} \neq 0 \text{ and } HW(\mathbf{u}) \text{ is even} \\ n & \text{otherwise, i.e., if } \mathbf{u} \neq \mathbb{1} \text{ and } HW(\mathbf{u}) \text{ is odd} \end{cases}.$$

Building an oracle out of HQC's C implementation

```c
typedef union {
  uint16_t u16[8];
} codeword;

typedef union {
  int16_t i16[128];
} expandedCodeword;

void expand_and_sum(expandedCodeword *dst, codeword src[]) {
  for (size_t part = 0; part < 8; part++) {
    for (size_t i = 0; i < 16; ++i) {
      dst->i16[(part << 4) + i] = src->u16[part] >> i & 1;
    }
  }
  // sum the rest of the copies
  ...
}
```

Figure: C code of the Reed-Muller `expand_and_sum` function's optimized version with no SIMD

From the C to the ASM: validation of the leakage

```
; Load from memory
lw t0, 0(a0)
; Right shift of i
srl t1, t0, r
; Bit extraction
andi t1, t1, 1
; Store the extracted
    bit into memory
sh t1, 0(a1)
```

Figure: Instruction flow of the bit extraction in `expand_and_sum`

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Extraction at i = 14

inst	t_1				
srl-	0	...	0	0	b_{14}
srl+	0	...	0	b_{15}	b_{14}

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Extraction at i = 14

inst	t_1				
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Extraction at i $<$ 14

inst	t_1				
srl-	0 ...	...	...	0	b_i
srl+	0 ... 0	b_{15}	...	b_{i+2}	b_{i+1}

Easiness of real-world microarchitecture

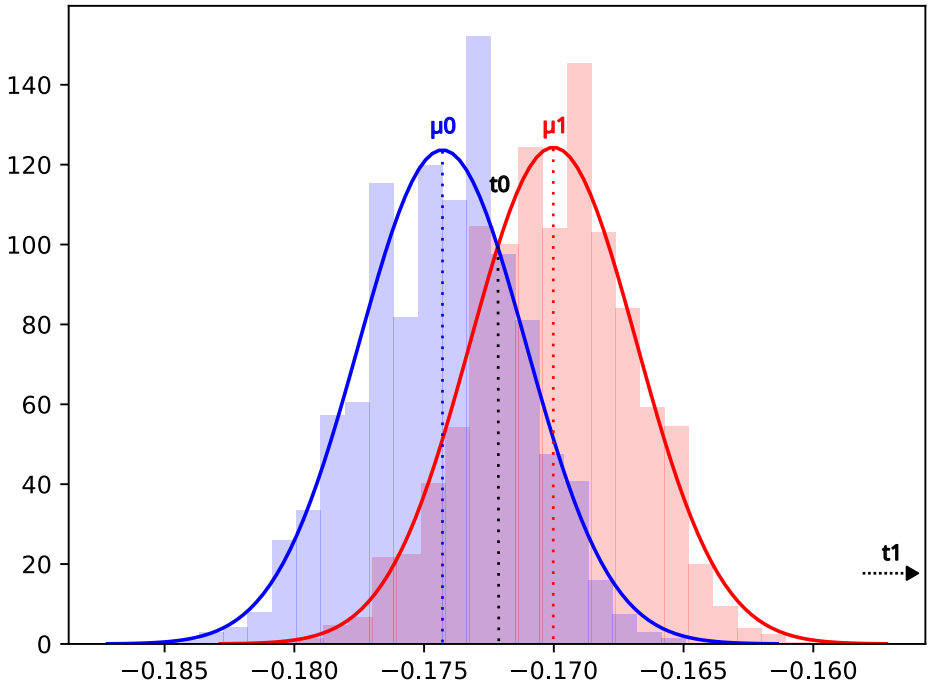

Figure: Power distributions for 0 and 1 on the point of interest for bit_0

Attack on Cortex-M4

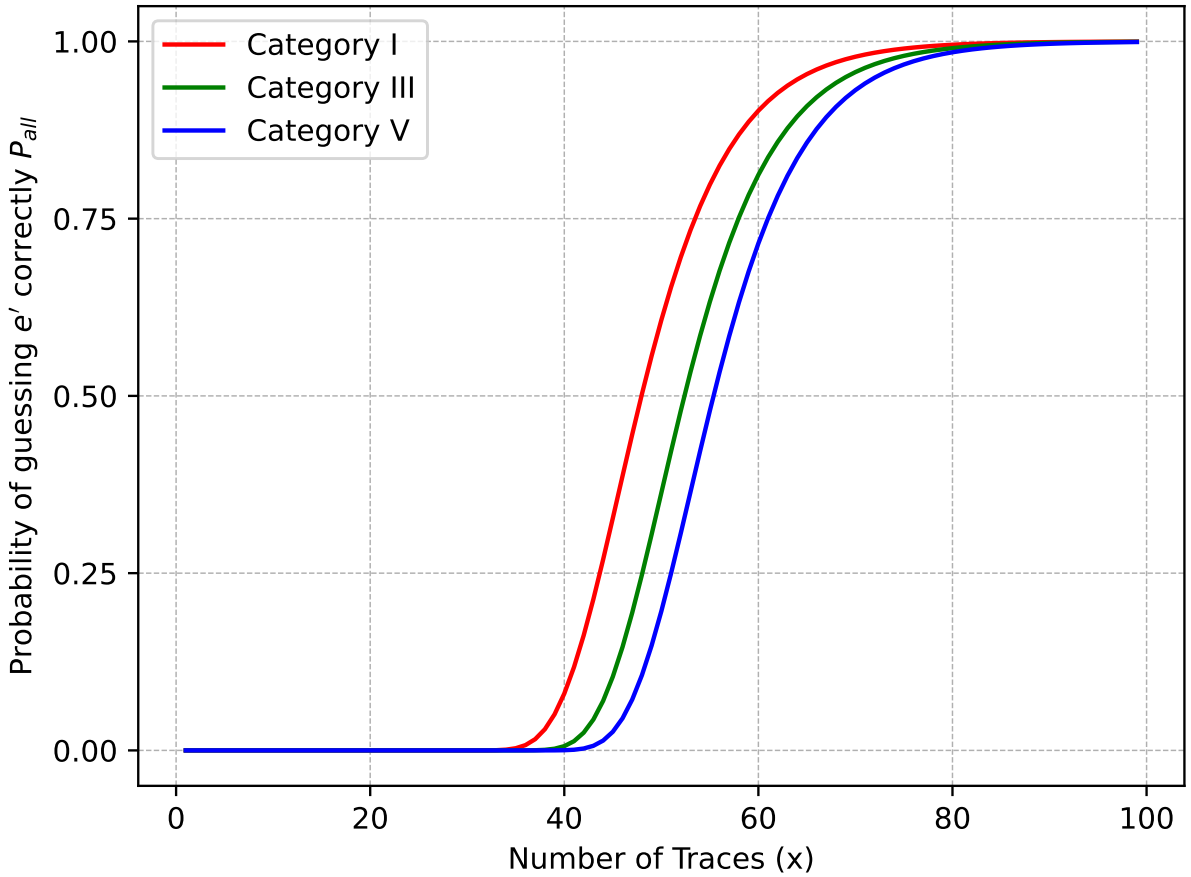

Figure: Probability of success of $(\mathbf{v} - \mathbf{u} \cdot \mathbf{y})$'s retrieval

Idea behind each countermeasure

Min. dist. decoder

Idea: Compare all (256) codewords to find the nearest to the input using the Hamming Distance.

As a result, an attacker can't peek on the result of $\mathbf{v} - \mathbf{u} \cdot \mathbf{y}$ as the `expand_and_sum` function does not exists anymore.

Idea behind each countermeasure

Min. dist. decoder

Idea: Compare all (256) codewords to find the nearest to the input using the Hamming Distance.

Adding noise

Idea: Add a random error $\mathbf{e}''$ of weight $\mathbf{w}_{\mathbf{e}''}$ such that $\binom{n}{\mathbf{w}_{\mathbf{e}''}} \gg 2^{128}$ to $\mathbf{v}$ before decoding.

As a result, peeking on the `expand_and_sum` function gives $(\mathbf{v} - \mathbf{u} \cdot \mathbf{y}) + \mathbf{e}'' = (\mathbf{mG} + \mathbf{e}') + \mathbf{e}''$.

Cat.	$\overline{HW(\mathbf{e}')}$	$w_{\mathbf{e}''}$	$\overline{HW(\mathbf{e}' + \mathbf{e}'')}$	DFR	DFR'
I	6003.93	11	6007.45	-132.86	-132.24

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Codeword masking

Idea: Encode a new (random) message $\mathbf{m}'$ and compute $\mathbf{v} + \mathbf{m}'\mathbf{G}$ before decoding.

As a result, reproducing the attacks "uselessly leaks" $\mathbf{v} - \mathbf{u} \cdot \mathbf{y} + \mathbf{m}'\mathbf{G}$.

Sum-up of the countermeasures

	Proposed countermeasures to prevent our attacks							
Min. dist. decoder	×	✓	×	×	✓	×	✓	✓
Adding noise	×	×	✓	×	✓	✓	×	✓
Codeword masking	×	×	×	✓	×	✓	✓	✓
Cycles ($\times 10^3$)	62875	66232	62963	63589	66320	63660	66929	67017
Overhead	0%	+5.34%	+0.14%	+1.14%	+5.48%	+1.25%	+6.45%	+6.59%

Table: Comparison to the reference implementation of the overhead of each countermeasure

Thank you for your attention

Acknowledgments

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